WHAT IS CLAIMED IS:

1. A method of accessing data storage locations in a memory circuit comprising the acts of:

issuing at least one memory access control signal to a first portion of said memory circuit; and

coupling a data bus to a second portion of said memory circuit in response to said at least one memory access control signal.

2. The method of Claim 1, wherein issuing at least one memory access control signal comprises issuing a row address strobe signal and a column address strobe signal.

3. The method of Claim 1, wherein issuing at least one memory access control signal comprises issuing a memory circuit enable signal.

4. The method of Claim 1, wherein coupling a data bus comprises closing a transfer gate in each line of said data bus.

5. A method of accessing data storage locations in a memory circuit comprising the acts of:

issuing at least one memory access control signal to a first portion of said memory circuit, the signal comprising a row address strobe signal and a column address strobe signal; and

coupling a data bus to a second portion of said memory circuit in response to said at least one memory access control signal, the coupling comprising closing a transfer gate in each line of said data bus.

6. A system for accessing data storage locations in a memory circuit comprising the acts of:

means for issuing at least one memory access control signal to a first portion of said memory circuit; and

means for coupling a data bus to a second portion of said memory circuit in response to said at least one memory access control signal.

7. The system of Claim 6, wherein the means for issuing at least one memory access control signal comprises means for issuing a row address strobe signal and a column address strobe signal.

8. The system of Claim 6, wherein the means for issuing at least one memory access control signal comprises means for issuing a memory circuit enable signal.

9. The system of Claim 6, wherein the means for coupling a data bus comprises means for closing a transfer gate in each line of said data bus.

10. A system for accessing data storage locations in a memory circuit comprising the acts of:

means for issuing at least one memory access control signal to a first portion of said memory circuit, the signal comprising a row address strobe signal and a column address strobe signal; and

means for coupling a data bus to a second portion of said memory circuit in response to said at least one memory access control signal, the coupling comprising closing a transfer gate in each line of said data bus.

11. A device for accessing data storage locations in a memory circuit comprising the acts of:

a component for issuing at least one memory access control signal to a first portion of said memory circuit; and

a component for coupling a data bus to a second portion of said memory circuit in response to said at least one memory access control signal.

12. The device of Claim 11, additionally comprising a component for issuing a row address strobe signal and a column address strobe signal.

13. The device of Claim 11, additionally comprising a component for issuing at least one memory access control signal comprises issuing a memory circuit enable signal.

14. The device of Claim 1, additionally comprising a component for coupling a data bus comprises closing a transfer gate in each line of said data bus.

15. A device for accessing data storage locations in a memory circuit comprising, the device comprising :

a component for issuing at least one memory access control signal to a first portion of said memory circuit, the signal comprising a row address strobe signal and a column address strobe signal; and

a component for coupling a data bus to a second portion of said memory circuit in response to said at least one memory access control signal, the coupling comprising closing a transfer gate in each line of said data bus.